CLAIM LISTING

1. (Currently Amended) A method for calculating pulse code modulated samples, said method comprising:

accessing an IMDCT sample from a previous set of IMDCT samples;

accessing an IMDCT sample from a present set of IMDCT samples;

calculating a first pulse code modulated sample from the accessed IMDCT sample from the previous set of IMDCT samples and the accessed IMDCT sample from the present set of IMDCT samples; and

calculating a second pulse code modulated sample from the accessed IMDCT sample from the previous set of IMDCT samples and the accessed IMDCT sample from the present set of IMDCT samples;

a second address register for

incrementing a first address register, said first register referencing a memory location in the first memory, the memory location in the first memory storing the IMDCT sample from the previous set of IMDCT samples; and

incrementing a second address register, said second register referencing a memory location in the second memory, the memory location in the second memory storing the IMDCT samples from the present set of IMDCT samples;

storing the first pulse code modulated sample in a memory location in a third memory; and

storing the second pulse code modulated sample in another memory location in the third memory

incrementing a third address register, said third register referencing the memory location in the third memory; and

decrementing a fourth address register, said fourth address register referencing the memory location in the third memory.

2. (Original) The method of claim 1, wherein calculating the second pulse code modulated sample comprises inverting the accessed IMDCT sample from the present set of IMDCT samples.

3. (Original) The method of claim 1, further comprising:

accessing a first inverse window coefficient; and

accessing a second inverse window coefficient.

4. (Original) The method of claim 3, wherein calculating the first pulse code modulated sample further comprises:

multiplying the accessed IMDCT sample from the previous set of IMDCT samples with the first inverse window coefficient; and

multiplying the accessed IMDCT sample from the present set of IMDCT samples with the second inverse window coefficient.

5. (Original) The method of claim 4, wherein calculating the second pulse code modulated samples further comprises:

accessing a third inverse window coefficient; and

accessing a fourth inverse window coefficient.

6. (Original) The method of claim 5, further comprising:

multiplying the accessed IMDCT sample from the previous set of IMDCT samples with a third inverse window coefficient; and

multiplying the accessed IMDCT sample from the present set of IMDCT samples with a fourth inverse window coefficient.

7. (Currently Amended) A system for calculating pulse code modulated samples, said method comprising:

a first address register for accessing an IMDCT sample from a previous set of IMDCT samples;

a second address register for accessing an IMDCT sample from a present set of IMDCT samples; ~~and~~

an arithmetic logic unit for calculating a first pulse code modulated sample from the accessed IMDCT sample from the previous set of IMDCT samples and the accessed IMDCT sample from the present set of IMDCT samples and calculating a second pulse code modulated sample from the accessed IMDCT sample from the previous set of IMDCT samples and the accessed IMDCT sample from the present set of IMDCT samples; and

a first memory for storing a portion of the previous set of IMDCT samples, the portion of the previous set of IMDCT samples comprising a last half of the previous set of IMDCT samples

a second memory for storing a portion of the present set of IMDCT samples, the portion of the present set of IMDCT samples comprising a first half of the present set of IMDCT samples;

a third memory for storing a plurality of inverse window coefficients;

a third address register for accessing a first one of the inverse window samples by decrementing; and

a fourth address register for accessing a second one of the inverse window samples by decrementing.

8. (Original) The system of claim 7, wherein the arithmetic logic unit calculates the second PCM sample by inverting the accessed IMDCT sample from the present set of IMDCT samples.

9-11. (Cancelled).

11. (Currently Amended) The system of claim 7 ~~10~~, further comprising:

~~a third address register for accessing a first one of the inverse window samples by decrementing;~~

~~a fourth address register for accessing a second one of the inverse window samples;~~

a fifth address register for accessing a third one of the inverse window samples; and

a sixth address register for accessing a fourth one of the inverse window samples;

12. (Original) The system of claim 11, wherein the arithmetic logic unit multiplies the accessed IMDCT sample from the previous set of IMDCT samples with the first inverse window coefficient and multiplies the accessed IMDCT sample from the present set of IMDCT samples with the second inverse window coefficient.

13. (Original) The system of claim 12, wherein the arithmetic logic unit multiplies the accessed IMDCT sample

from the previous set of IMDCT samples with the third inverse window coefficient and multiplies the accessed IMDCT sample from the present set of IMDCT samples with the fourth inverse window coefficient.

14. (Original) The system of claim 7, further comprising:

a fourth memory for storing the first pulse code modulated sample and the second pulse code modulated sample.

15. (Currently Amended) A circuit for calculating PCM samples, said circuit comprising:

a processor for executing a plurality of executable instructions;

an instruction memory for storing the plurality of executable instructions, wherein execution of the executable instructions causes:

accessing an IMDCT sample from a previous set of IMDCT samples from a first memory;

accessing an IMDCT sample from a present set of IMDCT samples from a second memory;

calculating a first pulse code modulated sample from the accessed IMDCT sample from the previous set of IMDCT samples and the accessed IMDCT sample from the present set of IMDCT samples; and

calculating a second pulse code modulated sample from the accessed IMDCT sample from the previous set of IMDCT samples and the accessed IMDCT sample from the present set of IMDCT samples;

wherein the processor further comprises:

a first address register for referencing a memory location in the first memory, the memory location in

the first memory storing the IMDCT sample from the previous set of IMDCT samples; and

a second address register for referencing a memory location in the second memory, the memory location in the second memory storing the IMDCT samples from the present set of IMDCT samples.

wherein execution of the plurality of instructions further causes:

incrementing the first address register; and

incrementing the second address register;

storing the first pulse code modulated sample in a memory location in a third memory; and

storing the second pulse code modulated sample in another memory location in the third memory

wherein the processor further comprises:

a third address register for referencing the memory location in the third memory; and

a fourth address register for referencing the memory location in the third memory

wherein execution of the plurality of instructions further causes:

incrementing the third address register; and

decrementing the fourth address register.

16-20. (Cancelled)

Please add the following claim:

--21. (New) The method of claim 1, wherein said IMDCT samples comprise reconstructed values from application of the Inverse Modified Discrete Cosine Transformation to modified discrete cosine transformation values.--